

PAGING MODE CONTROL METHOD AND APPARATUS

BACKGROUND OF THE INVENTION

5 1. Technical Field of the Invention

The present invention relates to a method and apparatus for controlling a paging mode wherein paging data are RAKE-received by a CDMA wireless telephone terminal.

2. Description of the Prior art

10 In a wireless telephone terminal, paging data reception is not continuously monitored in a paging mode in order to reduce a power consumption. More specifically, the wireless telephone terminal operates only a minimum circuit required for receiving paging data every paging cycle in which the base
15 station intermittently outputs paging data. Upon a completion of the reception of the paging data, the wireless telephone terminal switches off the paging mode and switches on a sleep mode in which a power supply for a receiving circuit for receiving the paging data is turned off. Every arrival of a
20 paging cycle, the wireless telephone terminal operates only a minimum circuit required for receiving paging data, and, upon completion of the reception of the paging data, the wireless telephone terminal repeats an operation for shifting the paging mode to the sleep mode.

25 In the sleep mode, only a circuit for measuring a paging cycle is operated. A system clock required for transmitting and receiving operations of the wireless telephone terminal has a high resolution and consumes electric power very much. Therefore, in order to measure the paging cycle, a paging clock

having a relatively low resolution and a small power consumption is used. For example, the paging clock is 32 kHz or 32.768 kHz.

In the sleep mode, an offset of a clock count having a low resolution is estimated. Therefore, a high resolution system clock is switched on before several pulses of the low resolution paging clock. Thus, the paging data are received on the basis of the system clock.

An excessive power consumed by about 31.25 μ sec to 100 μ sec corresponding to the time period of several clocks of 32 kHz can be neglected, because time required when the system clock starts to receive paging data is about 100 msec.

A next-generation portable wireless telephone system IMT 2000 employs the CDMA wherein transmission data are subjected to spread spectrum modulation by using a pseudo-noise code having a frequency bandwidth wider than that of the transmission data.

A signal transmitted from the base station is reflected and diffracted by mountains, buildings, and the like to reach a portable wireless terminal through a plurality of transmission paths. Therefore, the signal received by the portable wireless terminal consists of a plurality of waves. Therefore, as a receiving modulation system of the portable wireless terminal, a RAKE receiving system is used. In the RAKE receiving system, a received signal converted from a RF bandwidth to a base band is despread, so that a plurality of waves included in the received wave are separated. The separated signals are combined to obtain a demodulation output of the received signal.

692745-031001
TOP SECRET
A delay profile is formed to perform RAKE receiving, and a wireless transmission path is searched on the basis of the delay profile. The position of the searched transmission path must be subjected to RAKE combining. The delay profile is obtained
5 by plotting delay times of radio waves reaching a reception point on an abscissa, and plotting the powers of the radio waves on an ordinate. A delay profile forming range used for RAKE receiving is generally about several tens μ sec.

10 However, the rise up of a paging cycle measured by the paging clock does not occur simultaneously when the paging data arrive, because a paging clock having a low resolution is used to measure a paging cycle. In consideration of this error, the time range for forming the delay profile in the paging mode is 50 to 100 μ sec or less of the width of the paging clock plus
15 several tens μ sec which is a time range for forming a delay profile in the speech mode.

Further, in the paging mode, a memory size required for the delay profile must be several times larger than that required for a speech mode.

20

SUMMARY OF THE INVENTION

An object of the present invention is to provide a paging mode control method and apparatus which can more reliably RAKE-
25 receive paging data.

Another object of the present invention is to provide a paging mode control method and apparatus which can reliably RAKE-receive paging data and which does not have to increase a memory size.

6002745.00001

The paging mode control method of the present invention includes the steps of forming a delay profile, searching a path timing on the basis of the delay profile, and performing RAKE receiving on the basis of the path timing, the delay profile

5 includes a first delay profile formed by a mode and a second delay profile formed by a paging mode, and a range of the second profile is wider than a range of the first profile. When predicted time at which paging data are received is offset, the second delay profile having a range wider than the offset is

10 formed. For this reason, the paging data can be reliably RAKE-received.

The paging mode control method further includes the step of measuring a paging cycle of paging data intermittently originated by using a paging clock, and the range of the second

15 delay profile is larger than a cycle of the paging clock. When a paging cycle is measured by using the paging clock, an offset between the measurement result and an actual paging cycle is the cycle of the paging clock at most. For this reason, the range of the second delay profile is preferably equal to or larger

20 than the cycle of the paging clock.

The second delay profile is preferably formed by connecting the plurality of first delay profiles to each other. At this time, although a memory for recording the second delay profile requires a capacity which is several times a memory for

25 recording the first delay profile, it is better than that the paging data cannot be RAKE-received.

A resolution of the second delay profile is lower than a resolution of the first delay profile, the delay profile further includes a third delay profile formed by the paging mode, a

resolution of the third delay profile is equal to the resolution of the first delay profile, and the paging mode control method according to the present invention further includes the step of forming the third delay profile with respect to a range including
5 the path timing searched on the basis of the second delay profile. When the resolutions are made low as described above, even though an amount of information of the first delay profile and an amount of information of the second delay profile are equal to each other, the forming range of the second delay
10 profile is a wide range. More specifically, a memory for recording the delay profiles does not have to be increased to record the second delay profile.

The paging mode control apparatus of the present invention includes a delay profile calculation unit for forming a delay
15 profile, and a RAKE receiving demodulator for performing RAKE receiving on the basis of the delay profile, and the delay profile includes a first delay profile formed by a speech mode and a second delay profile formed by a paging mode, and a forming range of the second profile is wider than a forming
20 range of the first profile. When predicted time at which paging data are received is offset, the second delay profile having a range wider than the offset is formed. For this reason, the paging data can be reliably RAKE-received. At this time, when a paging cycle is measured by using a paging
25 clock, an offset between the measurement result and an actual paging cycle is the cycle of the paging clock at most. For this reason, the range of the second delay profile is preferably equal to or larger than the cycle of the paging clock.

The paging mode control apparatus of the present invention

092745-031001
TOP SECRET//SI//NF

further includes a paging mode control unit and a plurality of delay profile calculation units. The paging mode control unit notifies the plurality of profile calculation units of timings at which delay profiles are formed, respectively, and the plurality of delay profiles formed by the plurality of delay profile calculation units are preferably connected to each other to form the second delay profile. At this time, although a memory for recording the second delay profiles requires a capacity which is several times the capacity of a memory for recording the first delay profile, it is better than that the paging data cannot be RAKE-received.

The paging mode control apparatus of the present invention further includes a paging mode control unit for notifying the delay profile calculation unit of a resolution, the delay profile calculation unit forms the delay profile by the notified resolution, a resolution of the second delay profile is lower than a resolution of the first delay profile, the RAKE receiving demodulator searches a path timing on the basis of the second delay profile, the delay profile further includes a third delay profile formed by a resolution equal to that of the first delay profile in a paging mode, and the path timing is included in a range of the third delay profile. When the resolutions are made low as described above, even though an amount of information of the first delay profile and an amount of information of the second delay profile are equal to each other, the forming range of the second delay profile is wide. Therefore, the memory capacity needs not be increased for recording the second delay profile. Since the path timing searched on the basis of the second delay profile having a low

resolution is rough, the third delay profile is formed to search an exact path timing.

According to the present invention, paging data can be RAKE-received reliably.

5

BRIEF EXPLANATION OT THE DRAWINGS

FIG. 1 is a block diagram showing an embodiment of a paging mode control apparatus according to the present invention.

10 Fig. 2 is a flow chart showing the embodiment of a paging mode control method according to the present invention.

Fig. 3 is a timing chart related to the operation in Fig. 2.

Fig. 4 is a block diagram showing another embodiment of a paging mode control apparatus according to the present
15 invention.

Fig. 5 is a flow chart showing another embodiment of a paging mode control method according to the present invention.

Fig. 6 is a timing chart related to the operation in Fig. 5.

20 PREFERRED EMBODIMENT OF THE INVENTION

With reference to the accompanying drawings, in an embodiment of a paging mode control apparatus according to the present invention, a RAKE receiving demodulator is
25 arranged together with a paging mode control unit. The RAKE receiving demodulator 1, as shown in Fig. 1, is connected to a paging mode control unit 2. The paging mode control unit 2 has a system clock timing generation unit 3 and a paging cycle measurement unit 4. The RAKE receiving demodulator

1 has an antenna 5, receives a reception carrier signal from the antenna 5, and generates and outputs demodulation data.

The paging mode control unit 2 notifies the paging cycle measurement unit 4 of a paging cycle to instruct the paging cycle measurement unit 4 to start a paging cycle measurement. The paging cycle is a cycle in which a base station intermittently outputs paging data. The paging mode control unit 2 further instructs the system clock timing generation unit 3 to start or stop generation of a system clock. The paging mode control unit 2 further notifies the RAKE receiving demodulator 1 of an operation start timing at which a delay profile is formed to instruct the RAKE receiving demodulator 1 to perform a synchronous capturing method.

The system clock timing generation unit 3 generates a system clock, and supplies the system clock to the RAKE receiving demodulator 1. The system clock timing generation unit 3 further starts or stop the system clock by an instruction of the paging mode control unit 2. The system clock timing generation unit 3 further detects a system timing in a CDMA system from reception data, and output the system timing to the paging mode control unit 2.

The paging cycle measurement unit 4 has a paging clock. By an instruction for starting count of the paging mode control unit 2, the paging cycle measurement unit 4 notifies the paging mode control unit 2 of an elapse of the paging cycle when the paging cycle elapses from the instruction. The paging cycle is expressed by a count value "n" ("n" is a positive integer) of paging clocks.

The RAKE receiving demodulator 1 comprises a RF receiving

unit 6, despreading units 7 to 9, delay profile calculation units 11 to 13, a synchronous capturing unit 14, a data despreading unit 15, and a data demodulation unit 16. The RF receiving unit 6 receives a reception carrier signal from the antenna 5, converts the reception carrier signal into a baseband spread spectrum signal, and outputs the base band spread spectrum signal to the despreading units 7 to 9 to the data despreading unit 15.

The despreading units 7 to 9 generate correlation values on the basis of a forming timing of a delay profile notified by the paging mode control unit 2 and the base band spread spectrum signal. The despreading units 7 to 9 output the generated correlation values to the delay profile calculation units 11 to 13, respectively. The delay profile calculation units 11 to 13 generate delay profiles on the basis of the correlation values and the forming timing of the delay profile notified by the paging mode control unit 2. In a speech mode, only one delay profile calculation unit of the three delay profile calculation units 11 to 13 forms a delay profile. In a paging mode, the three delay profile calculation units 11 to 13 form delay profiles. The delay profile calculation units 11 to 13 output the generated delay profiles to the synchronous capturing unit 14.

The synchronous capturing unit 14 has a memory which can record three delay profiles, and records the three delay profiles output from the delay profile calculation units 11 to 13 in the memory. The synchronous capturing unit 14 further generates a path timing (selective path phase) on the basis of the three delay profiles and a synchronous capturing method designated by the paging mode control unit 2. The synchronous capturing

unit 14 outputs the generate path timing to the data
despreading unit 15. The data despreading unit 15 despread a
base band spread spectrum signal on the basis of the path
timing. The data demodulation unit 16 outputs the despread
5 base band spread spectrum signal to the data demodulation
unit 16. The data demodulation unit 16 demodulates the base
band signal, and outputs the demodulated data.

In this embodiment, the RAKE receiving demodulator 1 has
only one data despreading unit. However, a RAKE receiving
10 apparatus generally comprises a plurality of data despreading
units. When the RAKE receiving demodulator 1 comprises a
plurality of data despreading units, the synchronous capturing
unit 14 searches path timings the number of which is equal to
the number of data despreading units to set the path timings in
15 the data despreading units, respectively. In this manner, the
paging mode control apparatus according to the present
invention can also be executed with respect to a general RAKE
receiving apparatus.

Fig. 2 shows an operation of the paging mode control
20 apparatus according to the present invention in a paging mode.
The system clock timing generation unit 3 initially supplies a
system clock to the RAKE receiving demodulator 1. First, the
paging mode control unit 2 notifies the paging cycle
measurement unit 4 of a paging cycle before the paging mode is
25 set (step S1). The notified paging cycle is set as a cycle which
is shorter than an actual paging cycle by several clocks in
consideration of an offset of the count of the page clocks (step
S2). The paging timing is a timing at which reception of the
first paging data is completed.

After the paging timing is detected, the paging mode control unit 2 instructs the paging cycle measurement unit 4 to measure a paging cycle (step S3). The paging cycle measurement unit 4 starts to count paging clocks by an instruction from the paging mode control unit. The paging mode control unit 2 further instructs the system clock timing generation unit 3 to stop the system clock (step S4). The system clock timing generation unit 3 stops the system clock by an instruction from the paging mode control unit 2. The system clock is stopped to stop the function of the RAKE receiving demodulator 1, so that the RAKE receiving demodulation unit 1 is set a sleep mode. The order of step S3 and step S4 is not regarded. The processes may be performed while changing the order, and the processes may be simultaneously performed.

The paging cycle measurement unit 4 detects from a notification of measurement whether the paging cycle has elapsed or not (step S5). More specifically, after counting the paging clocks is started, the paging cycle measurement unit 4 detects whether the count value is n. When the count number is n, the paging cycle measurement unit 4 notifies the paging mode control unit 2 that the paging cycle has elapsed. In a sleep mode, the paging mode control unit 2 monitors notification of the paging cycle measurement unit 4.

The paging mode control unit 2 instructs the system clock timing generation unit 3 to start the system clock in response to notification of the elapse of the paging cycle. The RAKE receiving demodulator 1 returns from the sleep mode to the paging mode by the start of the system clock to start

preparation of paging data reception (step S6). After the
RAKE receiving demodulator 1 returns from the sleep mode,
the paging mode control unit 2 designates a forming timing for
forming a delay profile to the despreading units 7 to 9 and the
5 delay profile calculation units 11 to 13.

The paging mode control unit 2 further notifies the
synchronous capturing unit 14 of a synchronous capturing
method. More specifically, the most effective path timing is
detected from the three delay profiles respectively input from
10 the three delay profile calculation units 11 to 13 to instruct the
data despreading unit 15 to output the path timing.

The despreading unit 7 outputs a correlation value to the
delay profile calculation unit 11 by an instruction from the
paging mode control unit 2 on the basis of a base band spread
15 spectrum signal output from the RF receiving unit 6. The
delay profile calculation unit 11 calculates a delay profile from
the correlation value by an instruction from the paging mode
control unit 2, and outputs an operation result to the
synchronous capturing unit 14 (step S7).

20 The despreading unit 8 outputs a correlation value to the
delay profile calculation unit 12 by an instruction from the
paging mode control unit 2 on the basis of a base band spread
spectrum signal output from the RAKE receiving demodulator
1. The delay profile calculation unit 12 calculates a delay
25 profile from the correlation value by an instruction from the
paging mode control unit 2, and outputs an operation result to
the synchronous capturing unit 14 (step S8). A forming timing
designated at this time is a timing at which a delay profile
forming range has elapsed from a timing at which the delay

profile calculation unit 12 is designated. The delay profile forming range corresponds to the size of a memory in which a delay profile is recorded.

The despreading unit 9 outputs a correlation value to the
 5 delay profile calculation unit 13 by an instruction from the
 paging mode control unit 2 on the basis of a baseband spread
 spectrum signal output from the RAKE receiving demodulator
 1. The delay profile calculation unit 13 calculates a delay
 profile from the correlation value by an instruction from the
 10 paging mode control unit 2, and outputs an operation result to
 the synchronous capturing unit 14 (step S9). A forming timing
 designated at this time is a timing at which a delay profile
 forming range has elapsed from a timing at which the delay
 profile calculation unit 11 is designated.

15 The synchronous capturing unit 14 connects the three delay
 profiles to each other to record the connected delay profiles in a
 memory as a delay profile having a wide range. Since the wide
 range of the delay profile is larger than an offset between a
 paging cycle measured by the paging clock and a paging data
 20 arrival timing, the most effective path timing is reliably set
 within the wide range of the delay profile.

The synchronous capturing unit 14 searches the most
 effective path timing from the delay profile having the wide
 range to notify the data despreading unit 15 of the path timing
 25 (step S10). As the most effective path timing, a path timing
 having the largest correlation value is selected. A signal-to-
 interference ratio (SIR) of a reception signal, and a path timing
 having the best SIR is selected.

The data despreading unit 15 despreads a base band spread

spectrum signal input from the RF receiving unit 6 at a designated path timing, and outputs the base band signal to the data demodulation unit 16. The data demodulation unit 16 demodulates the base band signal (step S11). After the
5 demodulated data are outputted, it is decided whether the control operation must be out of the paging mode (step S12). When the control operation does not have to be out of the paging mode, the processes in step S3 to step S12 are repeated. After paging data are decoded, when the control operation must
10 be out of the paging mode, the RAKE receiving demodulator 1 is out of the paging mode and shifts to another mode.

The time chart in Fig. 3 shows paging data, a paging clock, a paging cycle counter value, the state of a system clock, and a delay profile forming timing. The paging clock is always
15 supplied to the paging cycle measurement unit 4. Initially, the RAKE receiving demodulator 1 is set in a state except for the paging mode, and the system clock is supplied to the RAKE receiving demodulator 1.

When the paging data are received, in a period of time from
20 time T1 at which the end of reception of paging data are detected to a trailing edge T2 of the first paging clock, a paging cycle counter value is started to be counted, and a system clock is stopped. A period of time from the end T1 of the reception of the paging data to the trailing edge T2 of the paging clock is
25 shorter than the cycle of the paging clock, and is shorter than a period of time which is three times the range of one delay profile.

The stop of the system clock shifts the RAKE receiving demodulator 1 to a sleep mode. With respect to the paging

cycle, a paging cycle counter value corresponds to $(n + 4)$, and the paging cycle measurement unit 4 notifies the paging mode control unit 2 of an elapse of the paging cycle before several clocks, e.g., before four clocks in this embodiment. More specifically, the paging cycle measurement unit 4 notifies the paging mode control unit 2 of the elapse of the paging cycle at a paging cycle counter value "n".

At time T3 at which the paging counter value is "n", the system clock is started. When the system clock is started, the control operation is out of the sleep mode, and the paging mode control unit 2 forms three delay profiles. At time T5 a delay profile range after time T4 at which forming the first delay profile of the three delay profiles is started, the second delay profile is formed. At time T6 a delay profile range after time T5, the third delay profile is formed. The three delay profiles are connected to each other. The connected delay profiles are used as a delay profile having a wide range.

A path timing is searched on the basis of the delay profile having the wide range, and paging data are RAKE-received and synthesized by the path timing. Upon completion of reception of the paging data, if the control operation does not have to be out of the paging mode, the system clock is stopped again, and the operation shifts to a sleep mode. When the RAKE receiving demodulator 1 must shift to a mode except for the paging mode, the RAKE receiving demodulator 1 shifts to the mode.

When the path timing is searched as described above, the path timing can be searched from the wide range, and the paging data can be more reliably RAKE-received. The

capacity of the memory of the RAKE receiving apparatus according to the present invention is three times the capacity of the memory of a conventional RAKE receiving apparatus. However, it is better that the capacity of the memory than that
5 paging data cannot be RAKE-received.

Fig. 4 shows another embodiment of a paging mode control apparatus according to the present invention. In another embodiment of the paging mode control apparatus according to the present invention, a RAKE receiving demodulator
10 comprises one despreading unit and one delay profile calculation unit, and is arranged together with a paging mode control unit. A RAKE receiving demodulator 31, as shown in Fig. 4, comprises a RF receiving unit 6, a data despreading unit 15, a data demodulation unit 16, a despreading unit 33, a delay
15 profile calculation unit 34, and a synchronous capturing unit 35. The RF receiving unit 6, the data despreading unit 15, and the data demodulation unit 16 correspond to the same parts in the previous embodiment, respectively, and operate in the same manners as in the previous embodiment.

20 A paging mode control unit 32 notifies a paging cycle measurement unit 4 of a paging cycle and instructs the paging cycle measurement unit 4 to start measurement of the paging cycle. The paging cycle is a cycle in which a base station intermittently outputs paging data. A paging mode control
25 unit 2 further instructs a system clock timing generation unit 3 to start or stop generation of a system clock. The paging mode control unit 2 further notifies the RAKE receiving demodulator 31 of an operation start timing of delay profile forming and an operational resolution, and designates a synchronous capturing

method. The operational resolution is a chip resolution or 1/4 chip resolution.

The despreading unit 33 generates correlation values on the basis of a baseband spread spectrum signal output from a RF receiving unit, an operation start timing notified by the paging mode control unit 32, and the operational resolution. The despreading unit 33 outputs the generated correlation values to the delay profile calculation unit 34.

The delay profile calculation unit 34 generates a delay profile on the basis of the correlation values, the operation start timing of the delay profile notified by the paging mode control unit 32, and the operational resolution. The delay profile calculation unit 34 outputs the generated delay profile to the synchronous capturing unit 35.

The synchronous capturing unit 35 has a memory which can record one delay profile, and generates a path timing on the basis of the delay profile and a synchronous capturing method designated by the paging mode control unit 32. The synchronous capturing unit 35 outputs the generated path timing to the data despreading unit 15 or the paging mode control unit 32. More specifically, the path timing generated from the delay profile formed at the chip resolution is output to the paging mode control unit 32, and the path timing generated from the delay profile formed at the 1/4 chip resolution is output to the data despreading unit 15.

Fig. 5 shows an operation of the paging mode control apparatus according to this embodiment in a paging mode. The system clock timing generation unit 3 initially supplies a system clock to a RAKE receiving demodulation unit 1. The

1002745-004034
paging mode control unit 32 notifies a paging cycle measurement unit 4 of a paging cycle before a paging mode is set (step S21). The paging cycle to be notified is set to be a paging cycle which is shorter than an actual paging cycle by several clocks in consideration of an offset of the count of paging clocks. The paging mode control unit 32 detects a paging timing (step S22).

When the paging timing is detected, the paging mode control unit 32 instructs the paging cycle measurement unit 4 to measure a paging cycle. The paging cycle measurement unit 4 starts to count paging clocks. The paging mode control unit 32 further instructs the system clock timing generation unit 3 to stop the system clock (step S23). The system clock timing generation unit 3 stops the system clock by an instruction from the paging mode control unit 2. The system clock is stopped to stop the function of the RAKE receiving demodulator 1, so that the RAKE receiving demodulation unit 1 is set a sleep mode.

The paging cycle measurement unit 4 detects from a notification of measurement whether the paging cycle has elapsed (step S24). More specifically, it is detected whether the count value is n after the count of the paging clocks is started. When the count value is n, the paging cycle measurement unit 4 notifies the paging mode control unit 32 that the paging cycle has elapsed. In a sleep mode, the paging mode control unit 32 monitors notification of the paging cycle measurement unit 4.

The paging mode control unit 32 instructs the system clock timing generation unit 3 to start the system clock in response to the notification of the elapse of the paging cycle. The RAKE receiving demodulator 31 returns from the sleep mode to the

0502745-054001

paging mode by the start of the system clock, and starts preparation of reception of paging data (step S25). After the RAKE receiving demodulator 31 returns from the sleep mode, the paging mode control unit 32 designates a forming timing for
5 forming a delay profile to the despreading 33 and the delay profile calculation unit 34, and instructs the despreading unit 33 and the delay profile calculation unit 34 to form a delay profile at the chip resolution.

The paging mode control unit 32 further notifies the
10 synchronous capturing unit 35 of a synchronous capturing method. More specifically, the most effective path timing is detected from the delay profile of the chip resolution, and the paging mode control unit 32 is instructed to output the path timing.

15 The despreading unit 33 generates a correlation value of the chip resolution at the forming timing obtained from the paging mode control unit 32, and outputs the generated correlation value to the delay profile calculation unit 34. The delay profile calculation unit 34 calculates the delay profile of the chip
20 resolution from the correlation value, and outputs an operation result to the synchronous capturing unit 35 (step S26). The synchronous capturing unit 35 records the delay profile in the memory.

25 The synchronous capturing unit 35 searches the most effective path timing from the recorded delay profile, and notifies the paging mode control unit 32 of the path timing (step S27). A probability that a path timing which is truly required exists near the rough path timing obtained as described above is high.

The paging mode control unit 32 instructs the despreading unit 33 and the delay profile calculation unit 34 to form a delay profile at the 1/4 chip resolution in a range including the notified path timing. By an instruction from the paging mode control unit 32, the despreading unit 33 and the delay profile calculation unit 34 form a delay profile at the 1/4 chip resolution (step S28). The delay profile formed at the 1/4 chip resolution is input to the synchronous capturing unit 35 again to search a path timing, and the synchronous capturing unit 35 searches the most effective path timing, and outputs the path timing to the data despreading unit 15 (step S29).

When the path timing is searched as described above, the path timing can be searched from a wide range, and paging data can be more reliably RAKE-received. In addition, the memory size of the synchronous capturing unit does not have to be increased.

The data despreading unit 15 inversely diffuses a baseband spread spectrum signal input from the RF receiving unit 6 at a designated path timing, and outputs the inversely diffused baseband spread spectrum signal to the data demodulation unit 16. The data demodulation unit 16 demodulates the despread baseband signal to output the demodulated signal (step S30). After the demodulated data are outputted, it is decided whether the control operation must be out of the paging mode (step S31). When the control operation does not have to be out of the paging mode, the processes in step S23 to step S31 are repeated. When the control operation must be out of the paging mode, the RAKE receiving demodulator 31 is out of the paging mode and shifts to another mode.

092745-084001
100180-547260

The time chart in Fig. 6 shows paging data, a paging clock, a paging cycle counter value, the state of a system clock, and a delay profile forming timing. In a period of time from time T10 at which the end of reception of paging data are detected to a leading edge T11 of the first paging clock, a paging cycle counter value is started to be counted, and a system clock is stopped. A period of time from the end T10 of the reception of the paging data to the trailing edge T11 of the paging clock is shorter than the range of the delay profile formed at the chip resolution.

The stop of the system clock shifts the RAKE receiving demodulator 1 to a sleep mode. With respect to the paging cycle, a paging cycle counter value corresponds to $(n + 4)$, and the paging cycle measurement unit 4 notifies the paging mode control unit 2 of an elapse of the paging cycle. At time T12 at which the paging counter value is "n", the system clock is started. When the system clock is started, the control operation is out of the sleep mode, and the paging mode control unit 2 starts to form a delay profile at the chip resolution (time T13). The most effective path timing of the delay profile is detected, and a delay profile near the path timing is formed at the 1/4 chip resolution (time T14).

A path timing is searched on the basis of the delay profile formed at the 1/4 chip resolution, and paging data are RAKE-received and synthesized by the path timing. Upon completion of reception of paging data, the system clock is stopped again, and the RAKE receiving demodulator 31 shifts to the sleep mode. When the operation must shift to other mode except for the paging mode, the operation shifts to the other mode.